What Is Claimed Is:

1. A liquid crystal display device having a COT structure array substrate, comprising:

a top gate type thin film transistor formed on a substrate and having an active layer, a gate electrode, a source electrode, and a drain electrode;

a storage capacitor adjacent to the top gate type thin film transistor and having a first storage electrode and a second storage electrode;

a black matrix on the top gate type thin film transistor;

a first pixel electrode at a pixel region and contacting the drain electrode;

a color filter on the first pixel electrode at the pixel region; and

a second pixel electrode on the color filter and contacting the first pixel electrode at a portion over the black matrix.

2. The device according to claim 1, further comprising a buffer layer between the top gate type thin film transistor and the substrate.

3. The device according to claim 1, further comprising a gate insulation layer between the active layer and the gate electrode and between the first storage electrode and the second storage electrode.

4. The device according to claim 3, further comprising an interlayer insulator on the gate insulation layer, wherein the interlayer insulator covers the gate electrode and the second storage electrode.

5. The device according to claim 4, wherein the gate insulation layer and the interlayer insulator have a first contact hole and a second contact hole, respectively, each of the first and second contact holes exposing a portion of the active layer.

6. The device according to claim 5, wherein the source electrode contacts the active layer through the first contact hole, and the drain electrode contacts the active layer through the second contact hole.

7. The device according to claim 1, further comprising a passivation layer on the drain electrode and the black matrix.

8. The device according to claim 7, wherein the passivation layer has a third contact hole exposing a portion of the drain electrode.

9. The substrate according to claim 8, wherein the passivation layer is formed beneath the first pixel electrode contacting the drain electrode through the third contact hole.

10. The device according to claim 1, wherein the black matrix is formed of an insulating material having a black color.

11. The device according to claim 1, wherein the black matrix is formed of black resin.

12. The device according to claim 1, wherein the active layer has an L-shape.

13. The device according to claim 1, wherein the active layer is formed of a polycrystalline silicon layer.

14. The device according to claim 13, wherein the polycrystalline silicon layer is doped except for a portion corresponding to the gate electrode.

15. The device according to claim 1, wherein the first storage electrode is connected to the active layer as a single layer.

16. The device according to claim 1, wherein the second storage electrode is parallel to the gate line.

17. A method of forming a liquid crystal display device having a COT structure array substrate, comprising:

forming a top gate type thin film transistor formed on a substrate and having an active layer, a gate electrode, a source electrode, and a drain electrode;

forming a storage capacitor adjacent to the top gate type thin film transistor and having a first storage electrode and a second storage electrode;

forming a black matrix on the top gate type thin film transistor;

forming a first pixel electrode at the pixel region and contacting the drain electrode;

forming a color filter on the first pixel electrode at the pixel region; and

forming a second pixel electrode on the color filter and contacting the first pixel electrode at a portion over the black matrix.

18. The method according to claim 17, further comprising forming a buffer layer between the top gate type thin film transistor and the substrate.

19. The method according to claim 17, further comprising forming a gate insulation layer on the active layer and the gate electrode and between the first storage electrode and the second storage electrode.

20. The method according to claim 19, further comprising forming an interlayer insulator on the gate insulation layer, wherein the interlayer insulator covers the gate electrode and the second storage electrode.

21. The method according to claim 20, wherein the gate insulation layer and the interlayer insulator have a first contact hole and a second contact hole, respectively, each of the first and second contact holes exposing a portion of the active layer.

22. The method according to claim 21, wherein the source electrode contacts the active layer through the first contact hole, and the drain electrode contacts the active layer through the second contact hole.

23. The method according to claim 17, further comprising forming a passivation layer on the drain electrode and the black matrix.

24. The method according to claim 23, wherein the passivation layer has a third contact hole exposing a portion of the drain electrode.

25. The method according to claim 24, wherein the passivation layer is formed beneath the first pixel electrode contacting the drain electrode through the third contact hole.

26. The method according to claim 17, wherein the black matrix is formed of an insulating material having a black color.

27. The method according to claim 17, wherein the black matrix is formed of black resin.

28. The method according to claim 17, wherein the active layer has an L-shape.

29. The method according to claim 28, wherein the active layer is formed of a polycrystalline silicon layer.

30. The method according to claim 17, wherein the polycrystalline silicon layer is doped except for a portion corresponding to the gate electrode.

31. The method according to claim 17, wherein the first storage electrode is connected to the active layer as a single layer.

32. The method according to claim 17, wherein the second storage electrode is parallel with the gate line.

33. The method according to claim 17, wherein the forming first and second pixel electrodes comprises,

depositing a first transparent layer over the substrate;

depositing a second transparent layer over the first transparent layer; and

patterning the first and second transparent layers at the same time.